REMARKS

Applicants appreciate the examination of the application that is evidenced by the Official Action of December 2, 2005. Applicants also appreciate the indication that Claims 20-21 recite allowable subject matter. In response to the Official Action, Claims 1-5, 10-17 and 20 have been canceled and independent Claim 18 was amended to include the recitations from dependent Claim 20. Thus, Claims 18-19 and 21 are now in condition for allowance. Applicants have also added new Claims 60-61. Thus, the sole outstanding issue is the patentability of original Claims 6-9 and new Claims 60-61.

Claims 6-9 and 60-61 are Patentable Over the Cited References

Applicants acknowledge that US 2004/0168019 to Barlow et al. discloses a memory array that can support reading and writing of horizontal and vertical data. (See, e.g., Barlow et al., FIGS. 8-9 and paragraph 0059). However, Barlow et al. explicitly states that the:

> "configuration [of FIGS. 8-9] cannot be used to transpose data. If data is written to the horizontal port, and read from the vertical port, the data read will not be the columns of the original data. To correct this, a shifter is preferably added onto the read and write data lines, or on to the bit lines, so that data is always shifted into the correct place when being written or read. The shifter would be operable in response to the index number of the word line that is activated, to cause corresponding shifting of the bits on the appropriate lines." (See, Barlow et al., paragraph 0059).

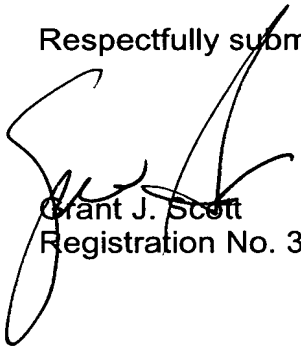
Applicants submit that this inability of the Barlow et al. configuration to "transpose" data is remedied by the use of "quad-port" cells as recited by independent Claims 6 and 60. Accordingly, the use of the "shifter" described by Barlow et al. can be eliminated. As noted by the Examiner, the use of "quad-port" cells is nowhere disclosed or suggested by Barlow et al. Moreover, although "quad-port" cells may be used as high bandwidth cells in many memory applications, as illustrated by FIGS. 3-4 of the present application and in Braceras et al. (US 5,561,781), Applicants submit that nowhere in any of the cited prior art

is there any disclosure or suggestion of using an array of quad-port cells to achieve a "transposition" between horizontal and vertical data, which is addressed by independent Claim 6.

Finally, Claims 60-61 recite the use of a data transfer control circuit which, as described at pages 9-10, 31 and 38-39 of the present application, can be used with multiple cache memory devices to "hide EDC latency" from FIFO read operations. This "hiding" of the EDC latency is achieved by switching back-and-forth between the multiple cache memory devices when performing "memory-to-cache" data transfer operations (e.g., from an external DRAM device to the FIFO controller). In particular, by switching back-and-forth, a "buffering" effect is achieved for FIFO read operations that effectively "hides" any timing delays associated with transferring data through EDC logic within the data transfer control circuit. Applicants submit that none of the cited prior art references disclose or suggest the subject matter of Claims 60-61.

Based on these arguments, Applicants respectfully submit that all pending claims are in condition for allowance, which is respectfully requested. **Applicants also respectfully request the Examiner to acknowledge receipt of an earlier amendment to correct inventorship (filed June 10, 2005).**

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 16, 2005.

Candi L. Riggs